REMARKS

Claims 1-53 are pending. Claims 1, 9, 16, and 24 have been amended. New claims 54-64 have been added. No new matter has been introduced. Reexamination and reconsideration of the present application are respectfully requested.

In the July 8, 2003 Final Office Action, the Examiner rejected claims 1-53. The Examiner rejected claims 1, 2, 7, 8, 16, 17, 22, and 23 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,182,257 to Gillingham (the Gillingham reference), in view of U.S. Patent No. 6,477,674 to Bates et al. (the Bates reference), in view of U.S. Patent No. 5,815,427 to Cloud et al. (the Cloud reference), and U.S. Patent No. 6,247,070 to Ryan et al. (the Ryan reference).

The Examiner rejected claims 3 and 18 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, in view of the Bates reference, the Cloud reference, and the Ryan reference, and further in view of U.S. Patent No. 5,638,382 to Krick et al. (the Krick reference).

The Examiner rejected claims 4 and 19 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Bates reference, the Cloud reference, and the Ryan reference, and the Krick reference, and further in view of U.S. Patent No. 4,837,785 to McAlpine (the McAlpine).

The Examiner rejected claims 5 and 20 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Bates reference, the Cloud reference, and the Ryan reference, the Krick reference, and further in view of U.S. Patent No. 5,633,878 to Ernkell et al. (the Ernkell reference).

The Examiner rejected claims 6 and 21 under 35 U.S.C. § 103(a) as being

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obvious over the Gillingham reference, the Bates reference, the Cloud reference, and the Ryan reference, the Krick reference, and further in view of U.S. Patent No. 5,835,936 to Tomioka et al. (the Tomioka reference).

The Examiner rejected claims 9, 10, 15, 24, 25, and 30 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, in view of the Cloud reference, and the Ryan reference.

The Examiner rejected claims 11 and 26 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Cloud reference, and the Ryan reference, and further in view of the Krick reference.

The Examiner rejected claims 12 and 27 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Cloud reference, and the Ryan reference, and the Krick reference, and further in view of the McAlpine reference.

The Examiner rejected claims 13 and 28 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Cloud reference, and the Ryan reference, and the Krick reference, and further in view of the Ernkell reference.

The Examiner rejected claims 14 and 29 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Cloud reference, and the Ryan reference, and the Krick reference, and further in view of the Tomioka reference.

The Examiner rejected claims 31, 32, 33, 36, 38, 39, 40, 41, 42, 45, and 47 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,415,403 to Huang et al. (the Huang reference), in view of U.S. Patent No. 5,946,247 to Osawa et al. (the Osawa reference), the Cloud reference, and the Ryan reference.

The Examiner rejected claims 34 and 43 under 35 U.S.C. § 103(a) as being

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obvious over the Huang reference, the Osawa reference, the Cloud reference, and the Ryan reference, and further in view of U.S. Patent No. 6,058,056 to Beffa et al. (the Beffa reference).

The Examiner rejected claims 35 and 44 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, the Osawa reference, the Cloud reference, and the Ryan reference, and further in view of U.S. Patent No. 6,019,501 to Okazaki (the Okazaki reference).

The Examiner rejected claims 37 and 46 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, the Osawa reference, the Cloud reference, and the Ryan reference, and further in view of U.S. Patent No. 5,883,843 to Hii et al. (the Hii reference).

The Examiner rejected claims 48-51 and 53 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, in view of the Osawa reference, the Beffa reference, and the Okazaki reference, the Cloud reference, and the Ryan reference.

The Examiner rejected claim 52 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, the Osawa reference, the Beffa reference, the Okazaki reference, the Cloud reference, and the Ryan reference, and further in view of the Hii reference. These rejections are respectfully traversed.

The present invention relates to a memory component, such as a DRAM device or a buffer device, residing within a memory module, having built-in self test. The memory component includes an input/output interface having a loopback. A controller is provided to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface. A compare

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register is provided to store and compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface. The memory module in which the memory component resides includes a plurality of memory devices and at least one buffer.

Amended Independent claim 1 recites:

A memory component with built-in self test, comprising:

an input/output interface having a loopback;

a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and

a compare register to store and compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

The Examiner rejected claims 1, 2, 7, 8, 16, 17, 22, and 23 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, in view of the Bates reference, the Cloud reference, and the Ryan reference).

The Gillingham reference is directed to a semiconductor device having a self test circuit that includes an embedded dynamic random access memory array for storing data. A self test controller is provided for internally generating test data patterns and expected resulting data, and for comparing the expected resulting data with actual resulting data. Test interface circuitry is provided for loading the test data patterns into the memory and reading back the actual resulting data from the memory. A

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programming circuit is provided for selectively programming a voltage level to be applied to a selected cell plate of the memory according to predetermined test requirements, and a storage circuit is provided for storing an address of a defective memory cell.

The Gillingham reference does not disclose, teach, or suggest the memory component of independent claim 1, as amended. As already acknowledged by the Examiner, the Gillingham reference "does not explicitly teach the specific use of a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and a compare register to store and compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface" (Office Action, page 3, paragraph No. 1). Moreover, unlike the memory component of independent claim 1, the Gillingham reference does not disclose a memory component comprising, among other things, a memory controller. The Gillingham reference shows that the **BIST controller (23) is external of the memory component (21)** that contains the memory array (DRAM) (38) therein (Col. 2, line 49-60; col. 3, lines 35-55; and Fig. 2). In other words, a memory component with built-in self test having an input/output interface, a controller, and a compare register, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer, as recited in independent claim 1, is different from the BIST system of the Gillingham reference in which the BIST controller is external to the memory component containing the memory array (DRAM) and not within a memory component residing in a memory module.

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The Bates reference does not make up for the deficiencies of the Gillingham reference. The Bates reference does not show a memory component with built-in self test having an input/output interface, **a controller**, and a compare register, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer, as recited in independent claim 1. The Examiner stated that "Bates et al., in analogous art, teach **I/O loopback tests are typically carried out** by providing data from a functional logic block (or FLB) within the IC (**e.g., a microprocessor**), and driving the data out through the output component of each I/O buffer (i.e., input/output interface). Subsequently, the data is driven back through the input component of the I/O buffer to the FLB in order to verify to that the correct data has been received. Consequently, the IC verifies whether the input and output components of each I/O buffer is functioning properly. (col. 1, lines 33-41, Bates et al.)"

The Applicants agree with the Examiner regarding Bates' stated reference to "typical" prior art loop back tests. However the Bates reference also states "The **problem with conventional I/O loopback tests**, however, is that generating and verifying test data patterns at the FLB require the addition of special logic within the FLB. Further, since the FLB is required to generate and check data, it is not possible to conduct other tests within the IC (e.g., the effect of I/O data on the FLB or vice versa). Therefore, **a method and apparatus for performing an I/O loopback test without using core logic within a FLB is desired** " (Col. 1, lines 42-50.) The Bates reference essentially teaches that it is undesirable to perform I/O loopback tests wherein a system processor (**e.g., a microprocessor**) performs the testing as is typically done. Therefore, the Bates reference does not teach the use of a controller. In fact, the Bates

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reference states "a method and apparatus for performing I/O loopback tests wherein I/O circuitry tests itself **independent of a system processor** is described". (Col. 2, lines 17-19.) The Bates reference shows in FIG. 1 that any signals from the core (e.g., a microprocessor) are external to the memory component, i.e., the I/O buffer 100.

The Bates reference also states "Stage unit 215 is coupled between test pattern generator 210 and compare unit 220 and receives test pattern signals from test pattern generator 210. According to one embodiment, **stage unit 215 provides a one cycle delay** for the test pattern signals before they are transmitted to compare unit 220 be compared with test signals received from amp 145. However, it will be appreciated that stage unit 215 may provide a higher magnitude of delay. Compare unit 220 is coupled to stage unit 215 and amp 145. Compare unit 220 compares test signals received from stage unit 215 with test signals received from amp 145, after having passed through the components of I/O buffer 100. If compare unit 220 detects a difference between the signals received from amp 145 and those received from test pattern generator 210, an error signal is transmitted from compare unit 220. According to one embodiment, compare unit 220 may be implemented using an Exclusive-Or-Gate. Alternatively, other comparison logic may be used to implement compare unit 220." (Col. 3, line 57-col. 4, line 9.) The Bates reference makes no mention of a compare register within the compare unit 220 for storing input/output test data. The Bates reference essentially teaches that the compare unit 220 (an exclusive-0R-gate or other comparison logic, but not a register) compares test signals received from stage unit 215 with test signals received from amp 145 in real time. The stage unit 215 provides **a one cycle delay** for

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the test pattern signals before they are transmitted to compare unit 220 be compared with test signals received from amp 145.

The Bates reference makes no mention of a controller or a compare register within a memory component, i.e., the I/O buffer 100. Therefore, the Bates reference does not show " A memory component with built-in self test, comprising: a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and a compare register to store and compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface".

Moreover, it is respectfully submitted that it would not have been obvious to one skilled in the art to combine the teachings of the Gillingham reference and the Bates reference, as suggested by the Examiner. It is well settled that a reference must provide some motivation or reason for one skilled in the art (working without the benefit of applicant's specification) to make the necessary changes in the disclosed device. The mere fact that a reference may be modified in the direction of the claimed invention does not make the modification obvious unless the reference expressly or implicitly teaches or suggests the desirability of the modification. In re Kotzab, 55 U.S.P.Q.2d 1313, 1317-18 (Fed. Cir. 2000); In re Fitch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Mills, 16 U.S.P.Q.2d 1430, 1432 (Fed. Cir. 1990).

The cited references, i.e., the Gillingham and the Bates references, fail to meet the basic requirement for a finding of obviousness established by the courts in Kotzab, Fitch, and Mills. There is no suggestion in either reference of modifying the memory component with built-in self test disclosed in the Gillingham reference in the direction of

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the present application, i.e., "a memory component with built-in self test having an input/output interface, a controller, and a compare register", nor is there any suggestion of the desirability of such modification.

Based on the Applicants' specification and claims, the Examiner is combining different references which are unrelated to each other, and none of which contains any teaching to be combined with each other.

The Bates reference, the Cloud reference, and the Ryan reference, alone or in combination, do not make up for the deficiencies of the Gillingham reference. In short, none of the Bates reference, the Cloud reference, and the Ryan reference discloses, teaches, or suggests a memory component with built-in self test having an input/output interface, a controller, and a compare register, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer, as recited in independent claim 1, as amended. Accordingly, applicants respectfully submit that independent claim 1, as amended, distinguishes over the above-cited references.

Amended Independent claim 16 recites limitations similar to independent claim 1, as amended. Claims 2-8 all depend, directly or indirectly, from independent claim 1, as amended. Claims 17-23 all depend, directly or indirectly, from amended independent claim 16. Accordingly, applicants respectfully submit that claims 2-8, and 17-23 distinguish over the above-cited references for the reasons set forth above with respect to independent claim 1, as amended.

Amended Independent claim 9 recites:

A memory component with built-in self test, comprising:

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a memory array;

an input/output interface coupled to the memory array and having a loopback;

a controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array; and

a compare register to store and compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

The Examiner rejected claims 9, 10, 15, 24, 25, and 30 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, in view of the Cloud reference, and the Ryan reference.

The Examiner stated in the office action that the Gillingham reference teaches a memory component and built-in self test, comprising: a controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array; and a compare register to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

The Examiner also stated "the compare register and the controller may be embodied within a single device or a common circuit (page 6, lines 12-13, specification of the present invention). The Applicants respectfully agree with the Examiner that the specification of the present invention describes the use of a controller and a compare

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register and states that "the compare register and the controller may be embodied within a single device or a common circuit". However, the Gillingham reference makes no mention whatsoever of a compare register much less a compare register and a controller embodied within a single device or a common circuit.

The Gillingham reference does not disclose, teach, or suggest the memory component of independent claim 9, as amended. Unlike the memory component of independent claim 9, as amended, the Gillingham reference does not disclose a memory component and built-in self test, comprising: a memory array; a controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array; and a compare register to store and compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

The Gillingham reference states "referring to FIG. 2, a block diagram illustrating the **main components** of the built-in self test and repair system according to an embodiment of the present system is shown generally by numeral 20.)" (Col. 3, line 34-37; and Fig. 2). FIG. 2 shows that the BIST controller (23) is external of the memory **component** (21) that contains the memory array (DRAM) (38) therein.

The Gillingham reference further states "the BIST controller 23 includes a data-in bus 27, an address bus 28 and control signals 29." Col. 3, lines 41-42.) The Gillingham reference makes no mention of a compare register in the BIST controller.

In other words, a memory component with built-in self test having a memory array, a controller, and a compare register, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer,

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as recited in independent claim 9, as amended, is different from the BIST system of the Gillingham reference in which the BIST controller is external to the memory component containing the memory array (DRAM) and the memory component is not within a memory module.

Neither the Cloud reference nor the Ryan reference make up for the deficiencies of the Gillinghm reference. Neither the Cloud reference nor the Ryan reference show a memory component with built-in self test having a memory array, a controller, and a compare register, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer, as recited in independent claim 9, as amended.

Claims 10-15 all depend, directly or indirectly, from independent claim 9, as amended. Accordingly, Applicants respectfully submit that claims 10-15 distinguish over the above-cited references for the reasons set forth above with respect to independent claim 9, as amended.

Amended Independent claim 24 recites limitations similar to independent claim 9, as amended. Claims 25-30 all depend, directly or indirectly, from amended independent claim 24. Accordingly, Applicants respectfully submit that claims 25-30 distinguish over the above-cited references for the reasons set forth above with respect to independent claim 9, as amended.

Independent claim 31 recites:

A memory module with built-in self test, comprising:

a plurality of memory components;

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an address and command buffer adapted to transmit address and command data and test data to one of the plurality of memory components, wherein the **address and command buffer includes a register to receive a test result**; and

at least **one data buffer to receive the test data from the address and command buffer, to receive the test data from the one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the one of the plurality of memory components to generate the test result**, wherein the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module.

The Examiner rejected claims 31, 32, 33, 36, 38, 39, 40, 41, 42, 45, and 47 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, in view of the Osawa reference, the Cloud reference, and the Ryan reference. The Examiner rejected claims 48-51 and 53 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, in view of the Osawa reference, the Beffa reference, and the Okazaki reference, the Cloud reference, and the Ryan reference. In so doing, the Examiner stated Huang et al. teaches a built-in self test for memory comprising "at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the one of the plurality of memory components to generate the test result (col. 4, lines 14-18, lines 31-33, Huang et al.)".

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The Huang reference is directed to a built-in self test (BIST) for an embedded memory. A BIST controller includes a finite state machine used to step through a test sequence and control a sequence controller. The sequence controller provides data and timing sequences to the embedded memory to provide page mode and non-page mode tests along with a refresh test. The BIST logic is scan-tested prior to performing the built-in self test and accommodations for normal memory refresh is made throughout the testing. The BIST also accommodates a burn-in test where unique burn-in test sequences can be applied.

The Huang references states " In FIG. 1 is shown a block diagram of the memory BIST 10 of this invention. The memory BIST 10 is comprised of a controller circuit 11 and **a sequencer circuit 12**. An embedded DRAM 13 is connected to a DRAM interface buffer 14 within the sequencer circuit. The DRAM interface buffer 14 connects data D, address ADDR, row access signal xRAS, column access signal xCAS, and write enable xWE to the embedded DRAM 13, and receives from the DRAM 13 data output Q. A sequence controller 15 receives commands and data from the controller circuit 11 and controls the row address counter 16 and the column address counter 17 to produce the appropriate address sequence exercise the DRAM 13 for the various march and burn-in tests. A control counter 18 is also controlled by the sequence controller 15 to produce the timing of signals from the timing generator 19 to control the timing sequence of signals connected to the DRAM 13 from the interface buffer 14. Data is transferred from the sequence controller 15 to the data composer 20 which inputs data D to the DRAM 13 through the interface buffer 14. Data form the data composer 20 is also connected to the **comparator 21** which received data out Q from

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the DRAM 13. The comparator compares the input data D from the data composer 20 to the output data Q from the DRAM 13 and outputs a go/no go signal BGO." (Col. 4, lines 11-33.) The **comparator 21** is in the **sequencer circuit 12** and not in the DRAM interface buffer 14. The comparator 21 receives data from the data composer 20 and does not receive data from an address command buffer. The data composer 20 receives data from the sequence controller 15. Neither the data composer 20 or sequence controller 15 are contained within a buffer.

Therefore, the Huang reference does not disclose, teach, or suggest the memory module of independent claim 31. Unlike the memory module of independent claim 31, the Huang reference does not disclose "at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the one of the plurality of memory components to generate the test result".

The Osawa reference, the Beffa reference, the Okazaki reference, the Cloud reference, and the Ryan reference, alone or in combination, do not make up for the deficiencies of the Huang reference. In short, none of the Osawa reference, the Beffa reference, the Okazaki reference, the Cloud reference, and the Ryan reference discloses, teaches, or suggests "at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the one of the plurality of memory components to generate the test result".

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As already acknowledged by the Examiner, "Huang et al. do not explicitly teach the specific use of a register to receive a test result" (Office Action, page 12, line 10). The Osawa reference does not make up for the deficiencies of the Huang reference. The Osawa reference is directed to a testing device for making a functional test on a semiconductor memory that is a logic integrated circuit including a plurality of RAMs, a plurality of ROMS, and the like.

The Osawa reference does not disclose, teach, or suggest the memory module of independent claim 31. Unlike the memory module of independent claim 31, the Osawa reference does not disclose "an address and command buffer adapted to transmit address and command data and test data to one of the plurality of memory components, wherein the **address and command buffer includes a register to receive a test result**".

The Osawa reference only teaches a self test circuit (702) that controls a register circuit (706) to receive test results from a RAM test conducted by the self test circuit (702) (col. 77, lines 62-64; and Fig. 142). The register circuit 706 is not in an address address and command buffer as required by independent claim 31. Accordingly, Applicants respectfully submit that independent claim 31, distinguishes over the above-cited references.

The Osawa reference, the Beffa reference, the Okazaki reference, the Cloud reference, and the Ryan reference, alone or in combination, do not make up for the deficiencies of the Huang reference. In short, none of the Osawa reference, the Beffa reference, the Okazaki reference, the Cloud reference, and the Ryan reference discloses, teaches, or suggests an address and command buffer adapted to transmit

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address and command data and test data to one of the plurality of memory components, wherein the **address and command buffer includes a register to receive a test result**; and at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the one of the plurality of memory components to generate the test result, as recited in independent claim 31. Accordingly, Applicants respectfully submit that independent claim 31, distinguishes over the above-cited references.

Independent claims 39 and 48, recite limitations similar to independent claim 31. Claims 32-38 all directly depend from independent claim 31. Claims 40-47 all depend, directly or indirectly, from independent claim 39. Claims 49-53 all directly depend from independent claim 48. Accordingly, applicants respectfully submit that claims 32-53 distinguish over the above-cited references for the reasons set forth above with respect to independent claim 31.

New claims 54-64 have been added to further define Applicants invention. Claims 54-64 distinguish over the Gillingham and Bates references for the reasons set forth above with respect to independent claim 1 and independent claim 16. Specifically, the Gillingham and Bates references do not show a memory component with built-in self test having an input/output interface, a controller, and a compare register. In addition, the Gillingham and Bates references do not show a controller to receive the memory array test data from the loopback of the input/output interface that was transmitted by the memory array to the input/output interface, and

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a compare register to store and compare the memory array test data transmitted to the memory array with the memory array test data received from the loopback of the input/output interface that was transmitted from the memory array, wherein the compare register generates a test result based the memory array test data transmitted to the memory array compared with the memory array test data received from the loopback of the input/output interface that was transmitted by the memory array to the input/output interface.

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Applicants believe that the foregoing amendments place the application in condition for allowance, and a favorable action is respectfully requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call either of the undersigned attorneys at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

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